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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	ATTORNEY DOCKET NO. CONFIRMATION NO.	
10/662,070	09/12/2003	Sergio Morini	2-3691	2-3691 9794	
2352	7590 02/20/20	04	EXAM	EXAMINER	
	K FABER GERB	CHANG, I	CHANG, DANIEL D		
_	NY 100368403	31.0	ART UNIT	PAPER NUMBER	
			2819	· · · · · · · · · · · · · · · · · · ·	

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No	D.	Applicant(s)				
	10/662,070		MORINI ET AL.				
Office Action Summary	Examiner		Art Unit				
	Daniel D. Char		2819				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address P riod for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). - Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status							
1) Responsive to communication(s) filed on 12.5	September 200:	3 .					
	nis action is non						
3) Since this application is in condition for allows closed in accordance with the practice under				nerits is			
Disposition of Claims							
4)⊠ Claim(s) <u>1-21</u> is/are pending in the application							
4a) Of the above claim(s) is/are withdraw	wn from conside	eration.					
5)⊠ Claim(s) <u>7-21</u> is/are allowed.							
6)⊠ Claim(s) <u>1-6</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/o	r election requir	rement.					
Application Papers	_						
9) The specification is objected to by the Examine			to boother Forestides				
10) The drawing(s) filed on <u>12 September 2003</u> is/a	,	•	•				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). 11) The proposed drawing correction filed on is: a) approved b) disapproved by the Examiner.							
If approved, corrected drawings are required in reply to this Office action. 12)☐ The oath or declaration is objected to by the Examiner.							
	armicr.						
Priority under 35 U.S.C. §§ 119 and 120	n nainaitu undaa	25 II Ó O S 140/o) (d) on (f)				
13) Acknowledgment is made of a claim for foreign	i priority under	35 U.S.C. 9 119(a)-(a) or (i).				
a) ☐ All b) ☐ Some * c) ☐ None of:							
1. Certified copies of the priority document			NI-				
2. Certified copies of the priority document							
3. Copies of the certified copies of the prio application from the International Bu* See the attached detailed Office action for a list	ıreau (PCT Rule	e 17.2(a)).		age			
14) Acknowledgment is made of a claim for domesti	e) (to a provisional a	pplication).					
a) ☐ The translation of the foreign language provisional application has been received.)☑ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachment(s)							
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	4) [5) [6) [Notice of Informal F	r (PTO-413) Paper No(s). Patent Application (PTO-1				

U.S. Patent and Trademark Office PTO-326 (Rev. 04-01) Art Unit: 2819

Drawings

The drawings are objected to because of the following errors:

In Fig. 2, a solid line above capacitor C should be a dotted line.

In Fig. 3, the input pulse 104 and input S of 102 should be separated in order to distinguish between a pulse and an input line.

In Fig. 4, right half of a solid line between P1 and P3 below 150 should be deleted, and the left half should be a dotted line similar to the dotted line connecting capacitor 152.

In Fig. 5, "N1" in lower right circuit should be replaced by --N3--.

In Fig. 6, the input pulse 196 and input N3 IN of 194 should be separated in order to distinguish between a pulse and an input line.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

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The disclosure is objected to because of the following informalities: for example, on page 2, line 18, the number "54" appears to be --52--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda (US 5,742,183).

Regarding claim 1, in figures 3A and 4A, Kuroda teaches a digital level shift circuit comprising:

a level shifting device (MN1) that is turned on to make an output transition (col. 5, lines 12-40); and

feedback circuitry (MN2, MP2) that obtains a feedback signal indicating that the level shifting device has made the output tranition and that turns off the level shifting device in response to the feedback signal (col. 5, lines 41-54).

Regarding claim 2, in figures 3A and 4A, Kuroda teaches that the level shifting device (MN1) receives a turn-on signal (when n4=VDDH) that turns on the device to make the output transition.

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Regarding claim 3, in figures 3A and 4A, Kuroda teaches that the output signal voltage range (does not necessarily mean minimum logic LOW to maximum logic HIGH voltage) extends from an offset voltage (VDDH-VDDL) to an upper voltage (VDDH) that is the sum of the offset voltage (VDDH-VDDL) and a fixed supply voltage (VDDH); and the offset voltage changing rapidly (more rapid than any slower changing voltage).

Regarding claim 4, in figures 3A and 4A, Kuroda teaches that the feedback circuitry includes a feedback device (either MN2/MP2 or MP1), the feedback device providing the feedback signal by turning on (either MN2 or MP1) when the level shifting device makes the output transition.

Regarding claim 5, in figures 3A and 4A, Kuroda teaches that one of the level shifting device (MN1) and the feedback device (either MP2 or MP1) is an n-channel device and the other is a p-channel device (col. 4, lines 62+).

Regarding claim 6, in figures 3A and 4A, Kuroda teaches that the n-channel and p-channel devices are high voltage MOS transistors (higher than any other lower voltage MOS transistors).

Allowable Subject Matter

Claims 7-21 are allowed.

Conclusion

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang Primary Examiner

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